GOVERNMENT POLYTECHNIC ,BARGARH
Department Of Electrical and ELECTRONICS Engineering

Semester: 3RD . DIPLOMA
Subject: DE LAB
Branch: EEE

Session: WINTER
No of Period :60(4p/week)
Name of Faculty: Niranjan Nayak

Week	Period	Topics to be Covered
1	1	Demonstration of Experiments of different types of gates and Combinational Circuits.
2	2	To verify the truth tables for all logic fates – NOT OR AND NAND NOR XOR XNOR using CMOS Logic gates and TTL Logic Gates.
3	3	Implement and realize Boolean Expressions with Logic Gates .
4	4	Implement Half Adder, Full Adder, Half Subtractor, Full subtractor using ICs.
5	5	Implement parallel and serial full-adder using ICs.
6	6	Design and development of Multiplexer and De-multiplexer using multiplexer ICs.
7	7	Demonstration of Experiments of different types of Flip-Flops , Counters , Shift registers , memory and converters
8	8	Verification of the function of SR, D, JK and T Flip Flops.
9	9	Design controlled shift registers.
10	10	Construct a Single digit Decade Counter (0-9) with 7 segment display.
11	11	To design a programmable Up-Down Counter with a 7 segment display.
12	12	Study of different memory ICs.
13	13	Study Digital- to – Analog and Analog to Digital Converters.
14	14	Simulate in Software (such as PSpice) an Analog to Digital Converter.
15	15	Simulate in Software (such as PSpice) a Digital to Analog Converter.